IN THE CLAIMS

Please amend the claims as follows:

Claims 1-6 (Canceled).

Claim 7 (Currently Amended): A processor comprising:

a processor core including a general-purpose register, an instruction decoder, and a second execution unit;

an extension unit including a first execution unit connected to the processor core; [[and]]

a direct memory access controller connected to the processor core and the extension unit; and

a control bus connected to both the processor core and the extension unit,

wherein the first execution unit is a reconfigurable first execution unit.

Claim 8 (Original): The processor of claim 7, wherein the extension unit further comprises an instruction decoder, a control register, and local memory.

Claim 9 (Currently Amended): The processor of claim 7, wherein ~~the instruction decoder in~~ the extension unit further comprises an instruction decoder comprising a reconfigurable logic circuit that is the same as the reconfigurable first execution unit.

Claim 10 (Currently Amended): The processor of claim 7, wherein configuration data ~~provided to the reconfigurable logic circuit,~~ is provided to the reconfigurable first execution unit through data transmission from the direct ~~access~~ memory access controller via a

configuration interface connecting the reconfigurable first execution unit in the extension unit and the direct memory access controller.

Claim 11 (Previously Presented): The processor of claim 8, wherein configuration data provided to the reconfigurable ~~logic circuit~~ first execution unit is stored in the local memory of the extension unit.

Claim 12-16 (Canceled).

Claim 17 (Currently Amended): A semiconductor integrated circuit, comprising:

a semiconductor chip;

a processor core integrated on the semiconductor chip including a general purpose register, an instruction decoder, and a second execution unit;

an extension unit integrated on the semiconductor chip including a first execution unit connected to the processor core;

a direct memory access controller integrated on the semiconductor chip and connected to both the processor core and the extension unit; and

a control bus integrated on the semiconductor chip and connected to both the processor core and the extension unit,

wherein the first execution unit is a reconfigurable first execution unit.

Claim 18 (Currently Amended): The semiconductor integrated circuit of claim 17, wherein ~~the instruction decoder in~~ the extension unit further comprises an instruction decoder comprising a reconfigurable logic circuit that is the same as the reconfigurable first execution unit.

Claim 19 (Currently Amended): The semiconductor integrated circuit of claim [[18]] 17, wherein configuration data provided to the reconfigurable ~~logic circuit~~ first execution unit, is provided through data transmission from the direct ~~access~~ memory access controller via a configuration interface connecting between the reconfigurable first execution unit in the extension unit and the direct memory access controller.

Claim 20 (Currently Amended): The semiconductor integrated circuit of claim 18, wherein configuration data provided to the reconfigurable ~~logic circuit~~ first execution unit is stored in the internal local memory of the extension unit.